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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Ashok Singhal, David J. Broniarczyk, George R. Cameron		
Assignee:	3PARdata, Inc.		
Amended Title:	Communication Link Protocol Optimized for Storage Architecture		
Serial No.:	09/751,649	Filing Date:	December 29, 2000
Examiner:	Steve N. Nguyen	Group Art Unit:	2133
Docket No.:	M-8495 US (3PD-M-8495 US)		

San Jose, California

Commissioner for Patents
P. O. Box 1450
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DECLARATION PURSUANT TO 37 C.F.R. § 1.132

Michel Cekleov declares and states as follows:

1. I have 21 years of experience as an electric engineer. I graduated with an Engineering degree (equivalent to a Master of Science) from Ecole Supérieure d'Ingénieurs de Marseille (France) in 1981. I also graduated with a doctorate degree in Electrical Engineering from Ecole Nationale Supérieure des Télécomunications (Paris, France) in 1986. After graduating, I worked at the research center of Thomson CSF (now Thales) for 4 years. More recently I worked at Sun Microsystems, Inc. as a system architect for 7 years and at Intel, Inc. as a system architect for 2 years. I currently work at 3PARdata, Inc. as a system architect.

2. I have reviewed U.S. Patent No. 6,049,889 ("Steely, Jr. et al."). Steely, Jr. et al. discloses a Memory Channel (MC) network of nodes with a reflected write feature. Each node in the MC network is a computer system with a memory divided into a local memory portion and a network memory portion. From col. 6, line 45 to col. 8, line 2, Steely, Jr. et al. discloses a second embodiment of the reflected write. In this embodiment of the reflected write, data is written to the

network memory portion of a sending node. In response, a MC adaptor at the sending node converts a local memory address of the sending node to a network memory address, and then transmits the data to a receiving node according to the network memory address. A MC adaptor at the receiving node receives the data and converts the network memory address to a local memory address of the receiving node. The MC adaptor then performs a direct memory access (DMA) operation to save the data to a local memory or an I/O device of the receiving node.

3. The DMA operation cited by the Examiner at col. 7, lines 29 to 33 is not a DMA write for writing a block of data from a local node to a remote node. Instead, the DMA operation is a local write from a local MC adaptor to a local memory or a local I/O device at the node.

4. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that theses statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the Application or any patent issued thereon.

Dated: October 31, 2005

Respectfully submitted,

Michel Cekleov